JAPAN UPDATE:
SDHPC
Strategic Direction/Development of HPC

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Disclaimer : Most information comes from public documents written in Japanese. English translations are not official.

Players and Major Project in Japan **at the last IESP**

Council for Science and Technology Policy (CSTP)

MEXT

MEXT : Ministry of Education, Culture, Sports, Science, and Technology

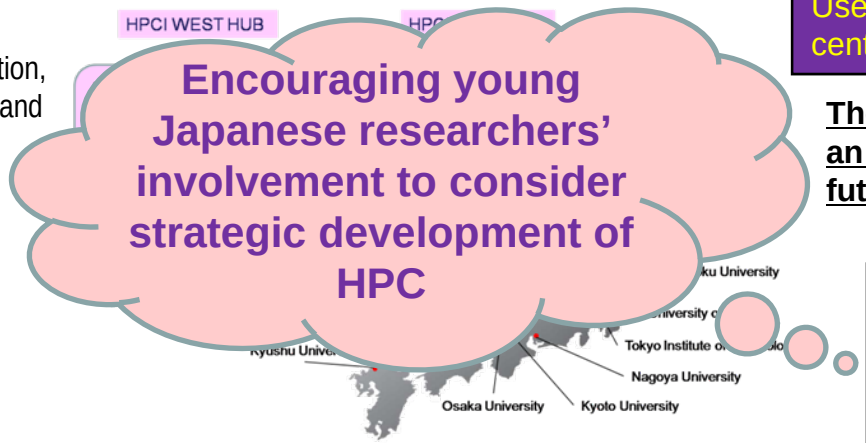
Council for HPCI Plan and Promotion

This is a council to Deputy Director-General, *Research Promotion Bureau at MEXT*

JST (Japan Science and Technology Agency)

HPCI Consortium established in 2012
Users and supercomputer centers (resource providers)

The consortium will play an important role of the future HPC R&D



Workshop of SDHPC (Strategic Development of HPC)
Organized by
- Univ. of Tsukuba
- Univ. of Tokyo
- Tokyo Institute of Tech.
- Kyoto Univ.
- RIKEN supercomputer center and AICS
- AIST
- JST

Basic Research Programs CREST: Development of System Software Technologies for post-Peta Scale High Performance Computing
2010 -- 2018

We already introduced this program at the last IESP

What Japan has been doing since the last IESP

MEXT : Ministry of Education, Culture, Sports, Science, and Technology

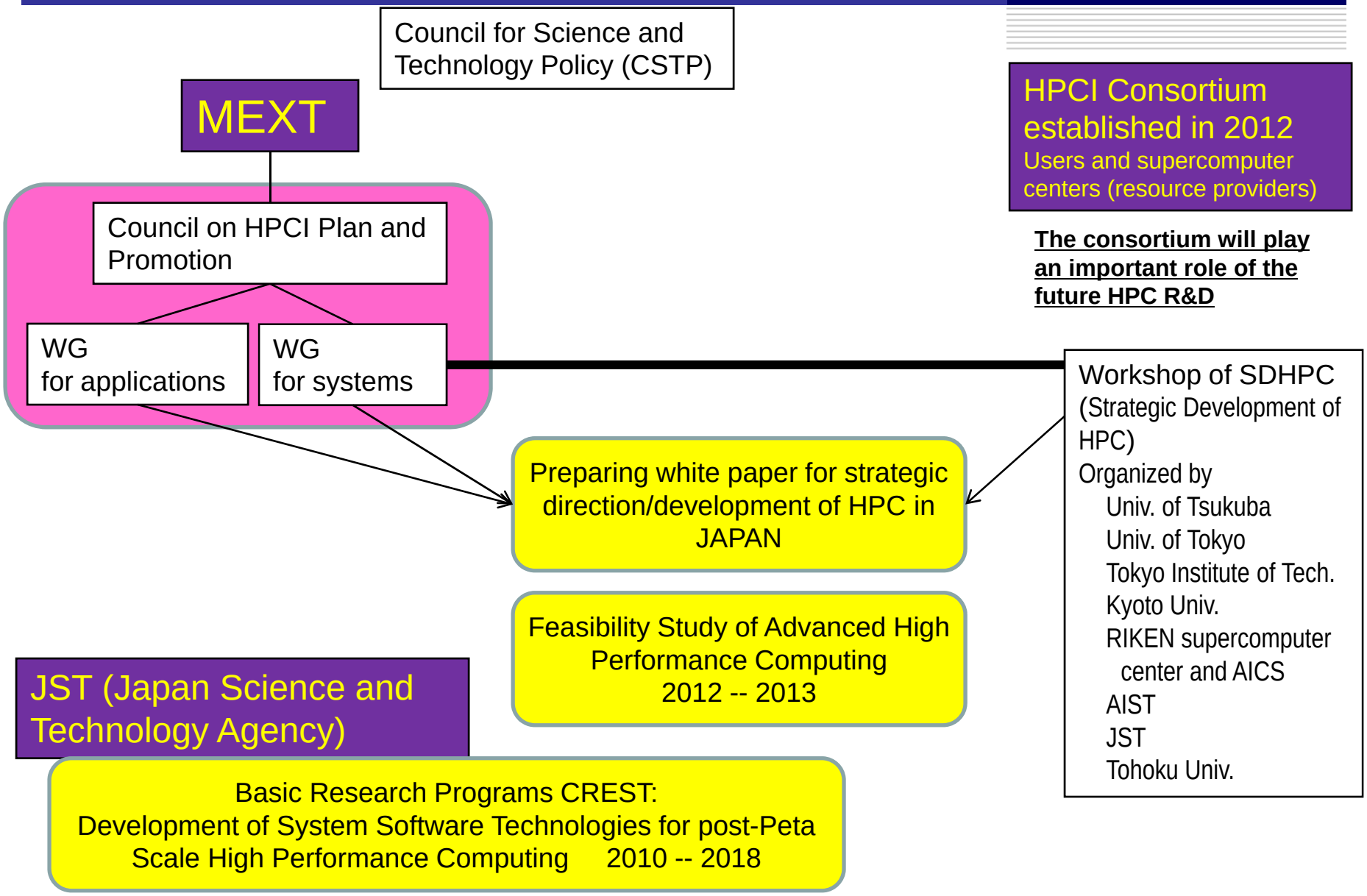
- MEXT organized a working group, discussing future development of HPC technologies, under the “Council for HPCI Plan and Promotion”

In other words, demonstrating scientific and technological values in exa-scale computing is very important for tax payers

The WG advised

- The first step should be discussion on how HPC technologies are applied to science and technology fields
- The system should be co-designed and developed with applications, computer architectures, and system software
- Several application-oriented computer architectures should be considered
- Prior to developing an exa-scale machine, tens to hundreds peta-scale machines should be deployed
- Strategic development, which pieces are developed in Japan and which pieces are internationally collaborated, should be determined
- The development of novel computational models and algorithms is also important
- The new application fields should be investigated

Players and Projects in Japan **NOW**



SDHPC

- White paper for Strategic Direction/Development of HPC in JAPAN is now being written by young Japanese researchers with advisers (seniors)
- The white paper will be approved by the Council for HPCI Plan and Promotion by the end of FY 2011.
- Contents (draft)
  - Expected scientific and technological values in exa-scale computing
  - Challenges towards exa-scale computing
  - Current research efforts in Japan and other countries
  - Approaches
  - Competitive vs Collaboration
  - Plan of R&D and organization
- The white paper will be used for call for proposals in “Feasibility Study of Advanced High Performance Computing”

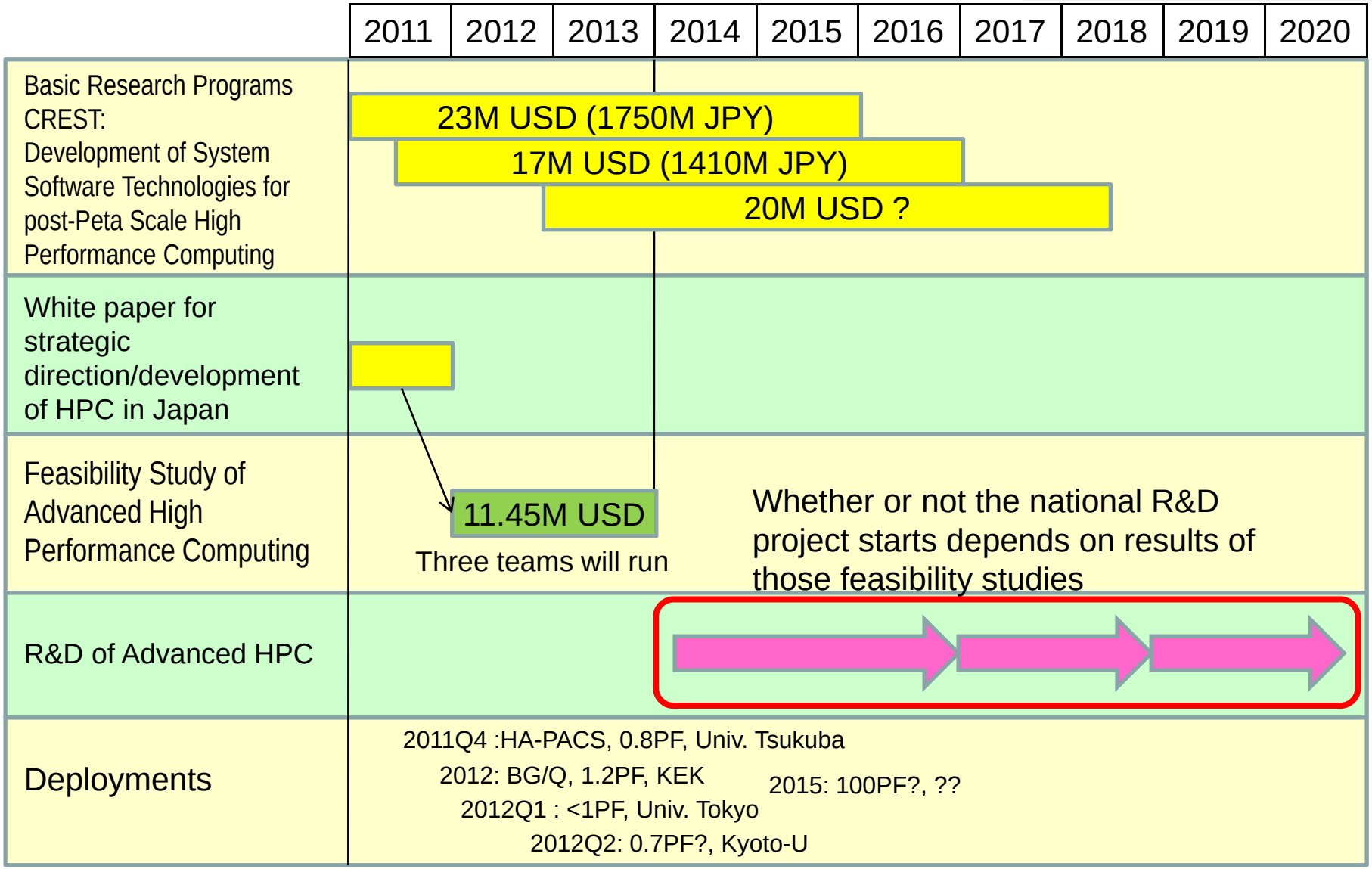
Feasibility Study of Advanced High Performance Computing

- MEXT (Ministry of Education, Culture, Sports, Science, and Technology) has just proposed two-year project for feasibility study of advanced HPC which will start in FY2012 (April of 2012)
- Objectives
  - The high performance computing technology is an important national infrastructure
  - Keeping development of top-level HPC technologies is one of Japanese international competitiveness and contributes national security and safety
  - This two-year project is to study feasibilities of such development that Japanese community should focus on
- Budget requested
  - 11.45M USD (859M JPY) / Year

Feasibility Study of Advanced High Performance Computing

- Plan
  - Several computer architectures will be selected based on their potential advantages in solving respective key socio-scientific problems in Japan Japan
  - For each system
    - Hardware trends are investigated
    - The system architecture and system software are designed (with applications and, its prototype system is developed)
  - As a result of this study, further R&D for Japanese HPC funded by the government is decided
- Organizations
  - Several R&D teams (maybe three) will be selected.

Plans


2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
Basic Research Programs
CREST:
Development of System Software Technologies for post-Peta Scale High Performance Computing
23M USD (1750M JPY)
17M USD (1410M JPY)
20M USD ?
White paper for strategic direction/development of HPC in Japan
Feasibility Study of Advanced High Performance Computing
11.45M USD
Three teams will run
Whether or not the national R&D project starts depends on results of those feasibility studies
R&D of Advanced HPC
Deployments
2011Q4 :HA-PACS, 0.8PF, Univ. Tsukuba
2012: BG/Q, 1.2PF, KEK
2012Q1 : <1PF, Univ. Tokyo
2012Q2: 0.7PF?, Kyoto-U
2015: 100PF?, ??

CREST: Development of System Software Technologies for post-Peta Scale High Performance Computing (1/3)

http://www.postpeta.jst.go.jp/en/

- Objectives
  - Co-design of system software with applications and post-peta scale computer architectures
  - Development of deliverable software pieces
- Research Supervisor
  - Akinori Yonezawa, Deputy Director of RIKEN AICS
- Run by JST (Japan Science and Technology Agency)
- Budget and Formation (2010 to 2018)
  - About 60M $ (47M$ in normal rate) in total
  - Round 1: From 2010 for 5.5 year (23M $ (1750M JPY))
  - Round 2: From 2011 for 5.5 year (17M $ (1410M JPY))
  - Round 3: From 2012 for 5.5 year (20M $?)

CREST: Development of System Software Technologies for post-Peta Scale High Performance Computing (2/3)

Round 1: From 2010 for 5.5 year

- Highly Productive, High Performance Application Frameworks for Post Petascale Computing
  - Naoya Maruyama, Tokyo Institute of Technology
- System Software for Post Petascale Data Intensive Science
  - Osamu Tatebe, University of Tsukuba
- ppOpen-HPC: Open Source Infrastructure for Development and Execution of Large-Scale Scientific Applications on Post-Peta-Scale Supercomputers with Automatic Tuning (AT)
  - Kengo Nakajima, University of Tokyo
- Parallel System Software for Multi-core and Many-core
  - Atsushi Hori, RIKEN AICS
- Development of an Eigen-Supercomputing Engine using a Post-Petascale Hierarchical Model
  - Tetsuya Sakurai, University of Tsukuba

CREST: Development of System Software Technologies for post-Peta Scale High Performance Computing (3/3)

Round 2: From 2011 for 5.5 year

- Development of a Numerical Library based on Hierarchical Domain Decomposition for Post Petascale Simulation
  - Ryuji Shioya, Toyo University
- Advanced Computing and Optimization Infrastructure for Extremely Large-Scale Graphs on Post Peta-Scale Supercomputers
  - Katsuki Fujisawa, Chuo University
- An evolutionary approach to construction of a software development environment for massively-parallel heterogeneous systems
  - Hiroyuki Takizawa, Tohoku University
- Development of Scalable Communication Library with Technologies for Memory Saving and Runtime Optimization
  - Takeshi Nanri, Kyushu University
- Software development for post petascale super computing --- Modularity for Super Computing
  - Shigeru Chiba, Tokyo Institute of Technology

Associated Post Petascale Projects

- Tokyo Institute of Technology
  - JSPS Grant-in-Aid for Scientific Research(S) “Billion-Way Parallel System Fault Tolerance”
    2011-15, Total 1.6 mil Euro
    - PI: Satoshi Matsuoka, Collaborators Franck Cappello (INRIA), Hideyuki Jitsumoto (U-Tokyo)
  - MEXT – Tokyo Tech “Ultra Green Supercomputing”
    2011-15 Total 2.6 mil Euro
    - PI: Satoshi Matsuoka
- Univ. of Tsukuba
  - HP PACS(Highly Accelerated Parallel Advanced system for Computational Sciences) project (2011 to 2013, total 4.0 mil Euro)
    - Objective: to investigate acceleration technologies for post-petascale computing and its software, algorithms and computational science applications, and demonstrate by building a prototype system
    - Design and deploy a GPGPU-based Cluster system
    - Research on programming model and languages, environment for parallel system with accelerators.
    - Design of Algorithms and applications for parallel system with accelerators.
    - Research on architectures for parallel system with accelerators.

Research activities in AICS RIKEN

- XcalableMP(XMP): A PGAS parallel programming model and language
  - Partners: AICS Programming environment research team and Univ of Tsukuba
  - The specification is proposed by a special interest group, XMP SPEC WG, organized in Japan PC Cluster consortium.
    - XMP extends C99 and Fortran 95 with directives, Co-array syntax, and user APIs.
    - XMP supports typical parallelization under global-view programming model. Many ideas on “global-view” programming are inherited from High Performance Fortran.
    - Co-arrray (both for Fortran and C) as local-view programming model
    - Other features: XMP-IO, MPI library interface, Accelerators/GPU extension (XMP-dev)
  - http://www.xcalablemp.org
- System Software for many-core architectures
  - Partners; AICS System software research team, Univ. of Tokyo, Tokyo Univ. of Argriculture and Technology, Kinki Univ, and Development WG in Japan PC Cluster consortium
  - Software packages will be distributed by Japan PC Cluster consortium
    - Micro kernel, smart message passing middleware, and I/O middleware