The Exceptional Challenges of Exascale Computing

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Agenda

- **Activities and investments in exascale**
- **Key challenges for achieving exascale**
- **Thoughts on the co-design process**
- **Working with the community**

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Activities and Investments

- **Intel Labs Europe**
  - **Exascale Computing Research Center**
  - **ExaCluster Laboratory**
  - **ExaScience Lab**
- **Universal Parallel Computing Research Center (UPCRC)**
  - *Client focus…*
- **Ubiquitous High Performance Computing (UHPC)**
- **Single-Chip Cloud Computer (SCC)**

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Investments – Intel Labs Europe

Exascale Computing Research Center, Paris

- **Participants**
  - Intel
  - CEA
  - GENCI
  - Université de Versailles Saint-Quentin-en-Yvelines
- **Research Agenda**
  - Programming models
  - Performance optimization and analysis
  - Application tuning and optimization

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Investments – Intel Labs Europe

ExaCluster Laboratory, Jülich

- **Participants**
  - Intel
  - Forschungszentrum Jülich
  - ParTec

- **Research Agenda**
  - System management
  - Software tools
  - Simulation

Investments – Intel Labs Europe

ExaScience Lab, Leuven

- **Participants**
  - Intel
  - Imec
  - U. Antwerp, Ghent U., Hasselt U., Katholieke U. Leuven, Vrije U. Brussel

- **Research Agenda**
  - Space weather application
 - Programming models
  - Power and reliability

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Investments – UPCRC

Universal Parallel Computing Research Center

- **Participants**
  - Intel
  - Microsoft
  - UCB
  - UIUC

- **Research Agenda** (relevant subset)
  - Deterministic languages
  - Scalable many core operations systems
  - Parallel correctness
  - Autotuners for linear algebra
  - Parallel patterns and frameworks

Investments – SCC

- **24 dual-core tiles**
- **6x4 mesh interconnect**
- **No cache-coherence between cores**
- **Message passing buffer**
- **Software-controlled frequency & voltage**
- **Choice of Linux or a few different research OSs.**
- **More than a cluster on a chip ... includes non-coherent memory**

Dual-core SCC Tile
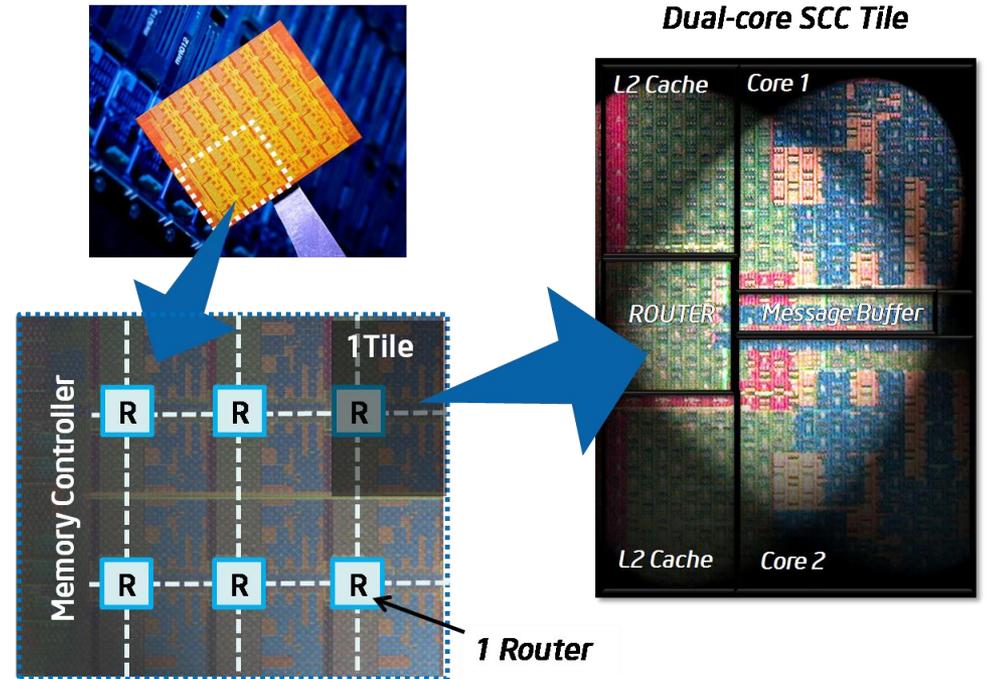
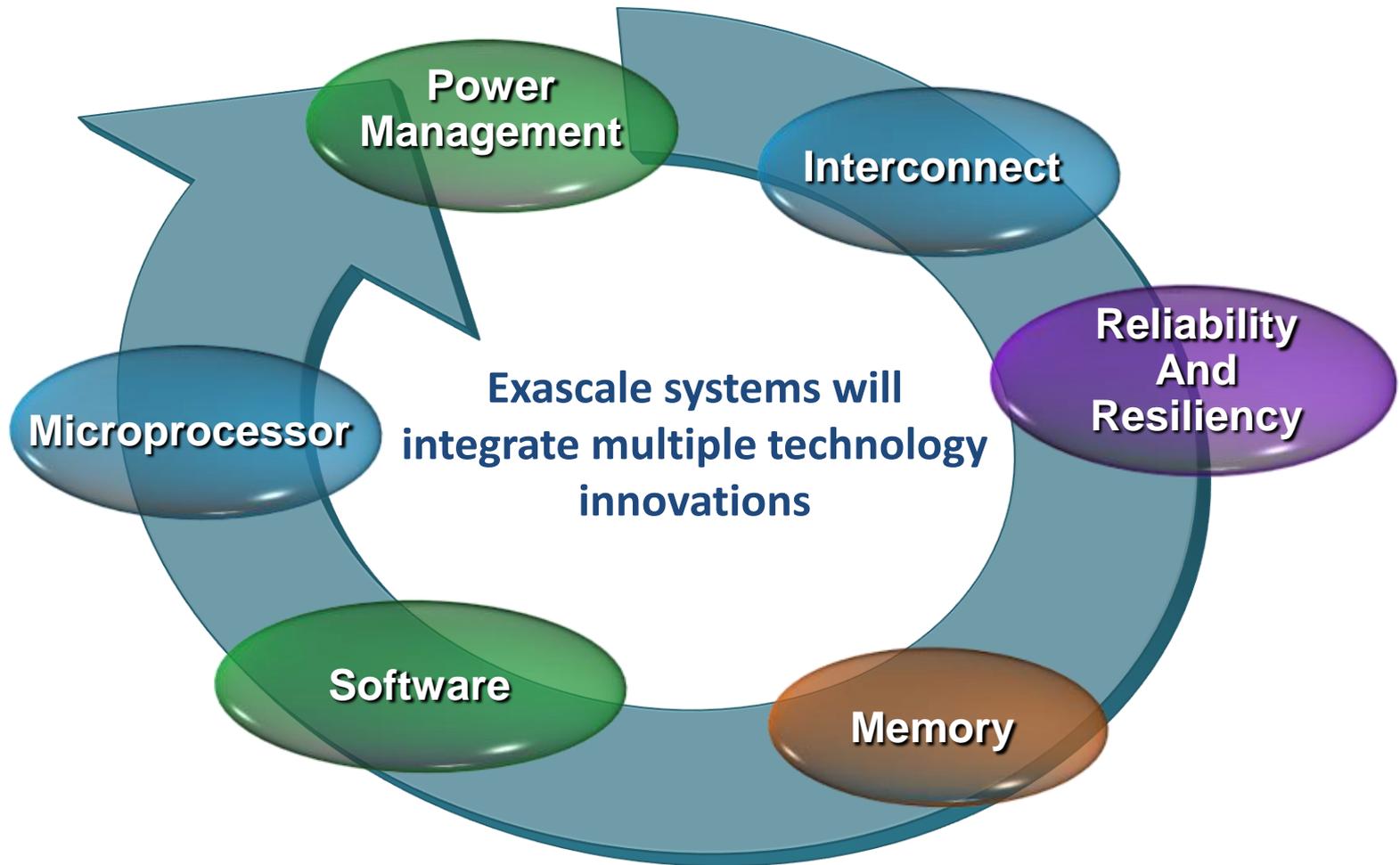| Technology	45nm Process
Interconnect	1 Poly, 9 Metal (Cu)
Transistors	Die: 1.3B, Tile: 48M
Tile Area	18.7mm²
Die Area	567.1mm²

The Path Forward

Research Needed to Achieve Exascale Performance

- Extreme voltage scaling to reduce core power
- More parallelism 10x – 100x to achieve speed
- Re-architecting DRAM to reduce memory power
- New interconnect lower power and distance
- NVM to reduce disk power and accesses
- Resilient design to manage unreliable transistors
- New programming tools for extreme parallelism
- Applications built for extreme parallelism

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Co-design is Essential

Power Management

Interconnect

Reliability And Resiliency

Microprocessor

Exascale systems will integrate multiple technology innovations

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Memory

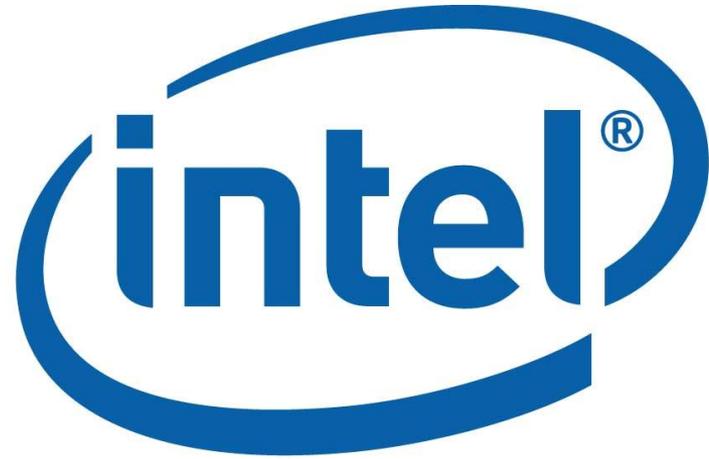**Co-design key to SCC, MIC, and our SoC products**

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Working with the Open Source Community

- **Intel contributes substantially to OSS**
  - Linux kernel, GNU tool chain, …
- **Intel's products focus on developer tools**
  - Compilers, MKL, MPI, correctness and performance tools, …
- **The OS, libraries, and runtime environment, programming models, other languages and tools, execution frameworks, resource managers, parallel file systems, &etc are all driven by or provided by vendors and the community**
- **Getting to exascale will provide substantial challenges**
  - New approaches will likely be required

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Backup

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OSS Contributors

- **Intel employs a large number of OSS maintainers and contributors**
  - **Kristen Carlson Accardi**
  - **H Peter Anvin**
  - **Len Brown**
  - **Alan Cox**
  - **Dirk Hohndel**
  - **Andi Kleen**
  - **Auke Kok**
  - **HJ Lu**
  - **Tony Luck**
  - **Venki Pallipadi**
  - **Inaki Perez-Gonzalez**
  - **Arjan van de Ven**
  - **Matthew Wilcox**
  - **David Woodhouse**
  - **and many more...**
- **In Linux 2.6 kernels, as of Oct 13, 2010:**
  - **11,048 patch sets by 258 Intel authors**

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