European Exascale Software Initiative

April 12, 2010

Oxford, UK

Jean-Yves Berthou

EDF

LEADING THE ENERGY CHANGE

European Exascale Software Initiative (EESI)

Context in Europe

HPC Eur - European High Performance Computing Initiative, "*The Scientific Case for a European Super Computing Infrastructure*", Petascale Computing in Europe - input for the ESFRI Roadmap process, spring 2006

DEISA, Distributed European Infrastructure for Supercomputing Applications

PRACE, Partnership for Advanced Computing in Europe **(PRACE)**

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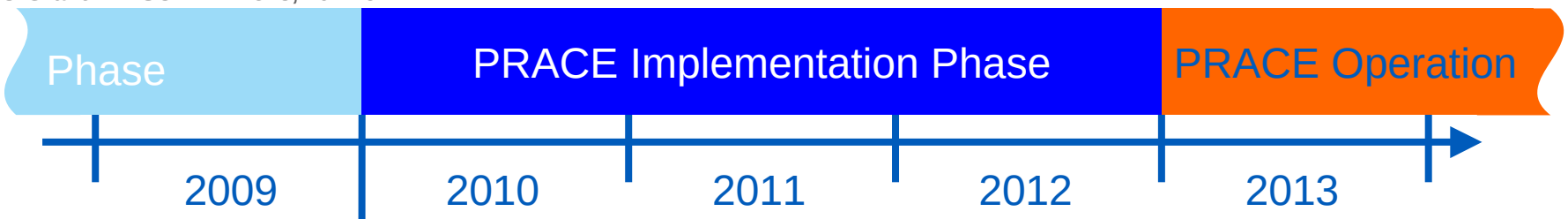
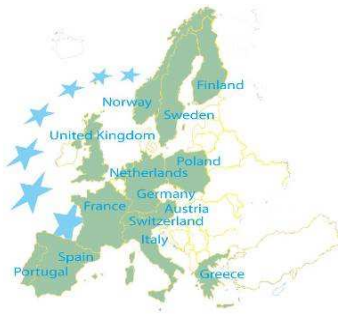
Context in Europe

PRACE History and first steps

EU-Grant: INFSO-RI-211528, 10 Mio. €





Foreseen: PRACE Tier-0 centres providing HPC-capability service in a legal entity

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Context in Europe

PRACE – A Partnership with a Vision

- Provide world-class HPC systems for word-class science
- Support Europe in attaining global leadership in public and private research and development

… and a Mission

- Create a world-leading persistent high-end HPC infrastructure managed as a single legal entity
  - Deploy 3 – 6 systems of the highest performance level (Tier-0)
  - IBM BlueGene/P in Jülich will be the first European Tier-0 system
  - Ensure a diversity of architectures to meet the needs of European user communities
  - Provide support and training

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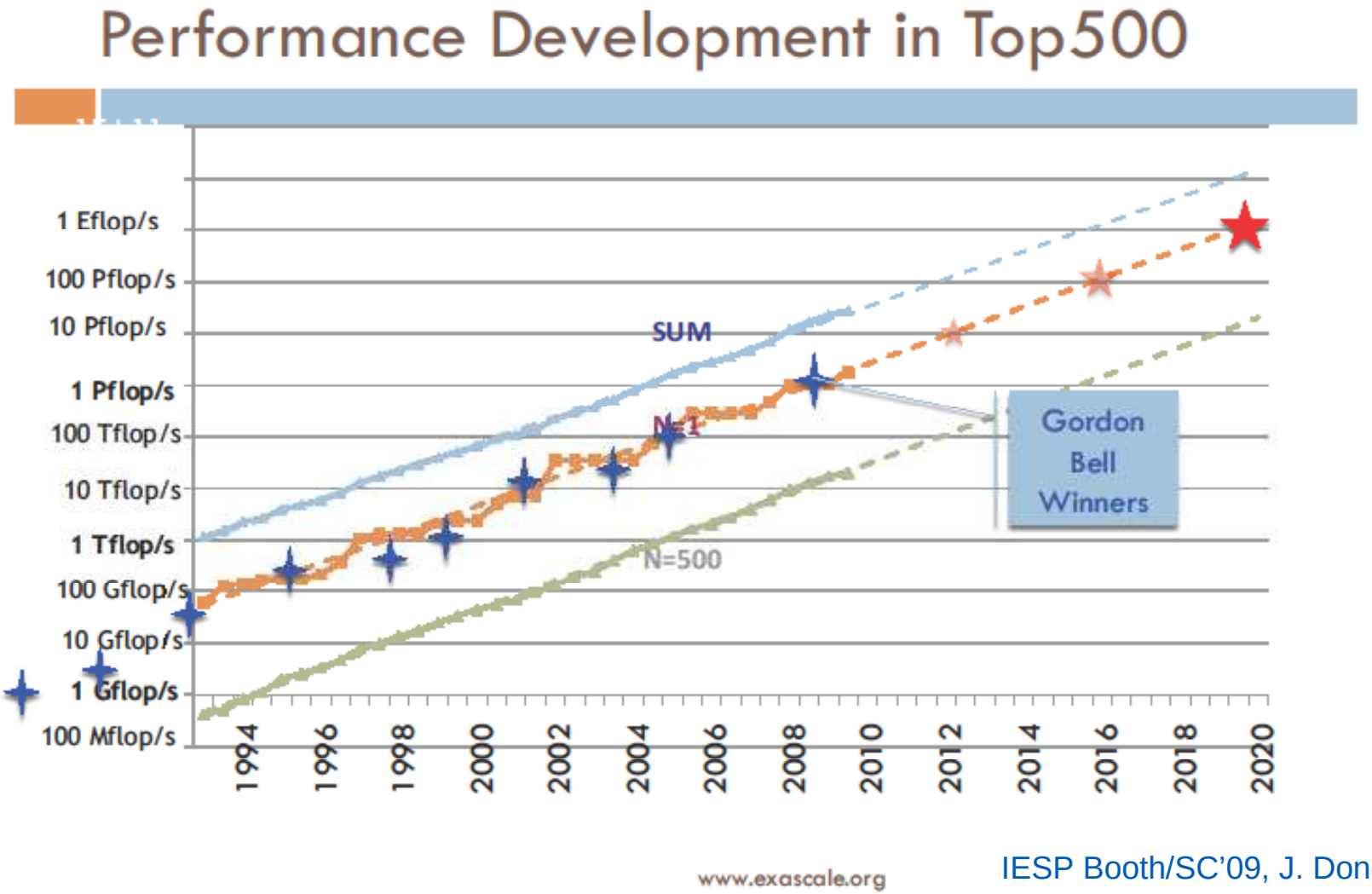

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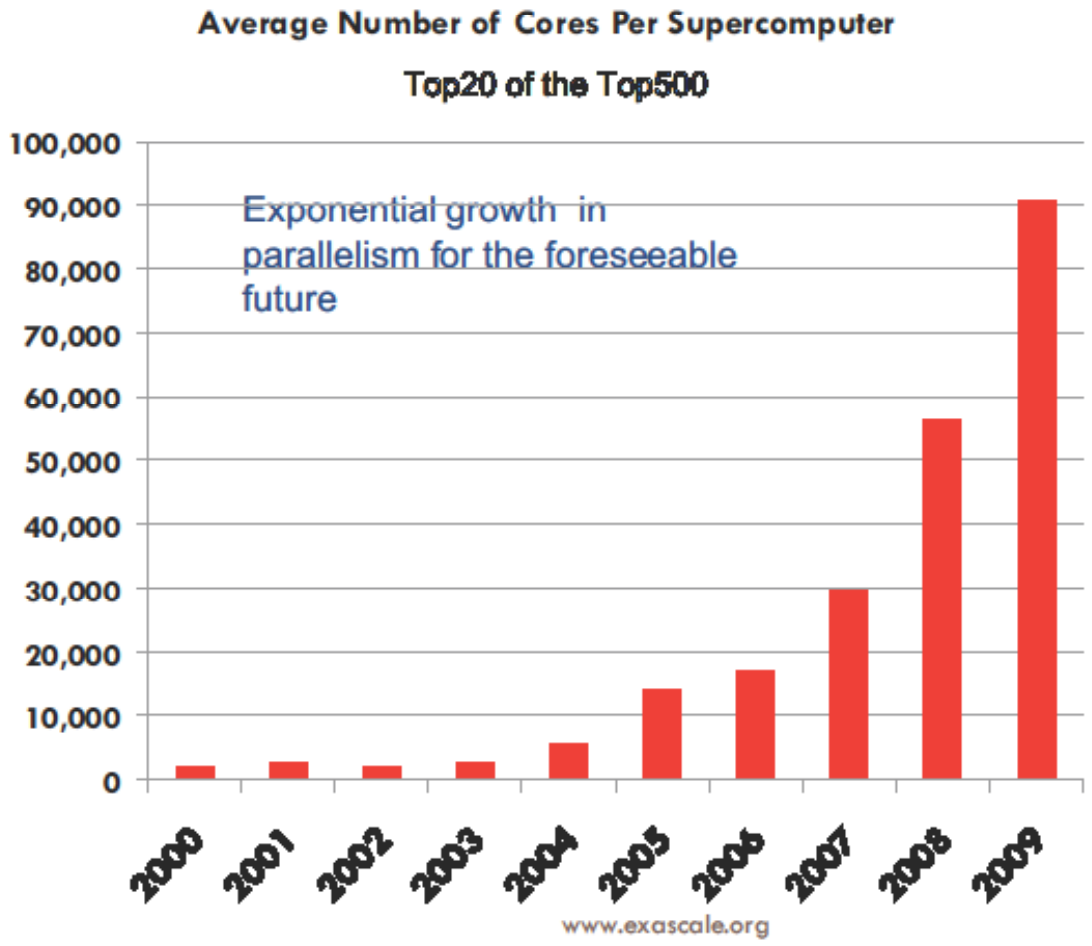

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Factors that Necessitate Redesign

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- **Steepness of the ascent from terascale to petascale to exascale**
- Extreme parallelism and hybrid design
  - Preparing for million/billion way parallelism
- Tightening memory/bandwidth bottleneck
  - Limits on power/clock speed implication on multicore
  - Reducing communication will become much more intense
  - Memory per core changes, byte-to-flop ratio will change
- Necessary Fault Tolerance
  - MTTF will drop
  - Checkpoint/restart has limitations

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- **Software infrastructure does not exist today**

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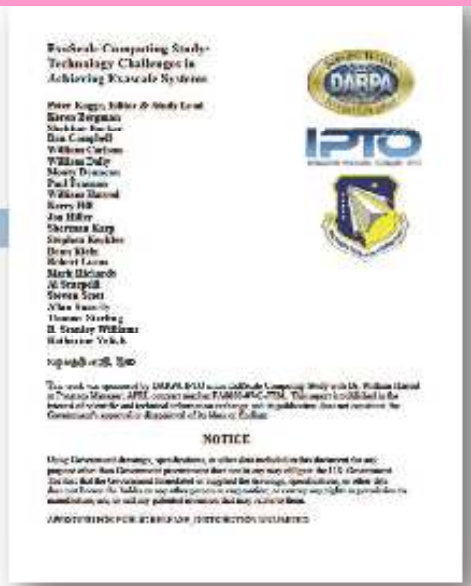
Exascale Computing



- Exascale systems are likely feasible by 2017±2
- 10-100 Million processing elements (cores or cores) with chips perhaps as dense as socket, clock rates will grow more slowly
- 3D packaging likely
- Large-scale optics based interconnects
- 10-100 PB of aggregate memory
- Hardware and software based fault management
- Heterogeneous cores
- Performance per watt — stretch goal 100 GF/watt of sustained performance ⇒ >> 10 – 100 MW Exascale system
- Power, area and capital costs will be significantly higher than for today's fastest systems

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Google: exascale computing study

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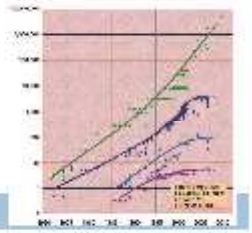
A Call to Action



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- Hardware has changed dramatically while software ecosystem has remained stagnant
- Previous approaches have not looked at co-design of multiple levels in the system software stack (OS, runtime, compiler, libraries, application frameworks)
- Need to exploit new hardware trends (e.g., manycore, heterogeneity) that cannot be handled by existing software stack, memory per socket trends
- Emerging software technologies exist, but have not been fully integrated with system software, e.g., UPC, Cilk, CUDA, HPCS
- Community codes unprepared for sea change in architectures
- No global evaluation of key missing components

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International Community Effort

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- We believe this needs to be an international collaboration for various reasons including:
  - The scale of investment
  - The need for international input on requirements
  - US, Europeans, Asians, and others are working on their own software that should be part of a larger vision for HPC.
  - No global evaluation of key missing components
  - Hardware features are uncoordinated with software development

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IESP Goal

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Improve the world's simulation and modeling capability by improving the coordination and development of the HPC software environment

Workshops:

Build an international plan for developing the next generation open source software for scientific high-performance computing

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Where We Are Today:

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- SC08 (Austin TX) meeting to generate interest — **Nov 2008**
- Funding from DOE's Office of Science & NSF Office of Cyberinfratructure and sponsorship by Europeans and Asians — **Apr 2009**
- US meeting (Santa Fe, NM) April 6-8, 2009
  - 65 people
- NSF's Office of Cyberinfrastructure funding — **Jun 2009**
- European meeting (Paris, France) June 28-29, 2009
  - 70 people
  - Outline Report
- Asian meeting (Tsukuba Japan) October 18-20, 2009
  - Draft roadmap
  - Refine Report — **Oct 2009**
- SC09 (Portland OR) BOF to inform others
  - Public Comment
  - Draft Report presented — **Nov 2009**

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Motivations for launching EESI

Coordinate the European contribution to IESP

Enlarge the European community involved in the software roadmapping activity

Build and consolidate a **vision and roadmap** at the European Level, including applications, both from academia and industry

European Exascale Software Initiative (EESI)

EESI main Goals

Build a **European vision and roadmap** to address the **challenge of performing scientific computing** on the new generation of computers which will provide multi-Petaflop performances in 2010 and Exaflop performances in 2020.

- Investigate how Europe is located, its strengths and weaknesses, in the overall international HPC landscape and competition
- Identify priority actions
- Identify the sources of competitiveness for Europe induced by the development of Peta/Exascale solutions and usages
- investigate and propose programs in education and training for the next generation of computational scientists
- Identify and stimulate opportunities of worldwide **collaborations**

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EESI main tasks

Coordination of the European participation in IESP

- *Make a thorough assessment of needs, issues and strategies*
- *Develop a coordinated software roadmap*
- *Provide a framework for organizing the software research community*
- *Engage and coordinate vendor community in crosscutting efforts*
- *Encourage and facilitate collaboration in education and training*

Cartography of existing HPC projects and initiatives in Europe, US and ASIA

Coordination of "*disciplinary working groups*" at the European level

- ***Four groups "****Application Grand Challenges"*
- ***Four groups "****Enabling technologies for Petaflop/Exaflop computing"*

Synthesis, dissemination and **recommendation** to the European Commission

European Exascale Software Initiative (EESI)

EESI expected outputs

A **roadmap** and **set of recommendations** to the funding agencies shared by the European HPC community, on software - tools, methods and applications - to be developed for this new generation of supercomputers.

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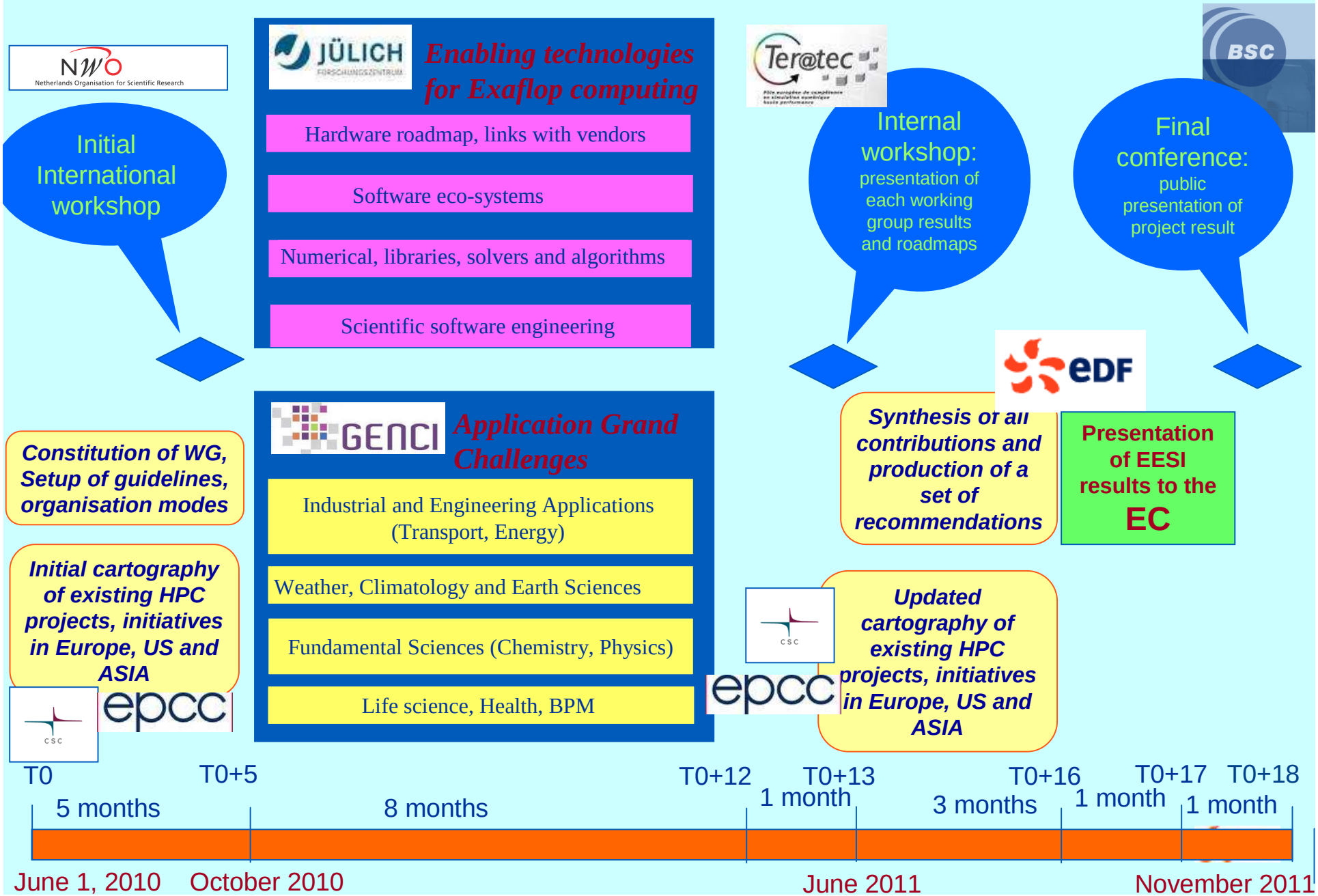

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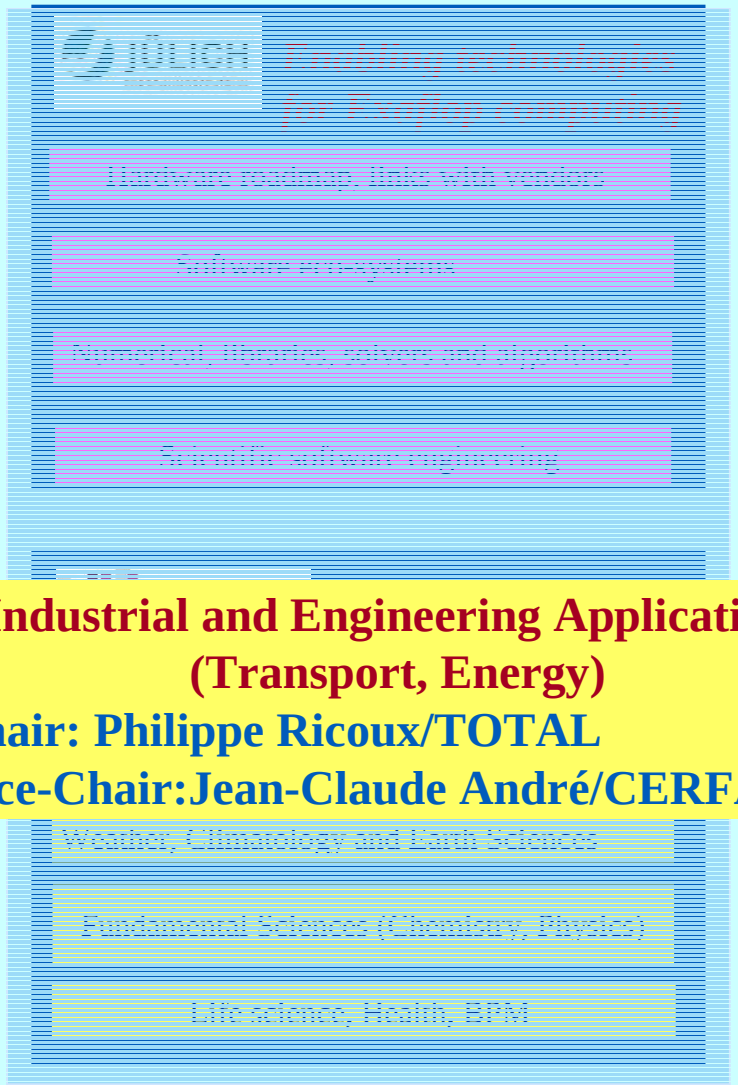
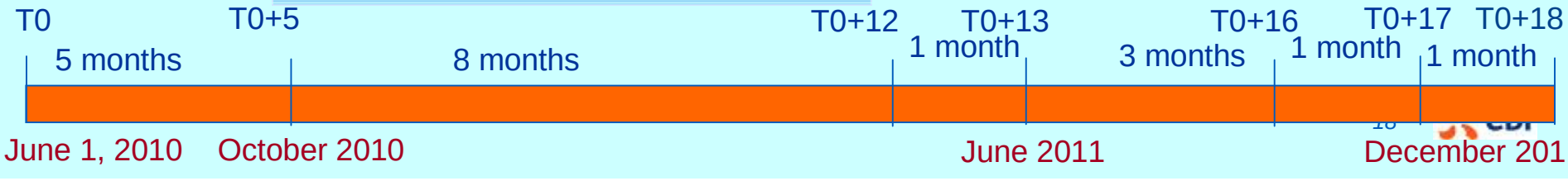


Industrial and Engineering Applications (Transport, Energy)

Chair: Philippe Ricoux/TOTAL

Vice-Chair:Jean-Claude André/CERFACS



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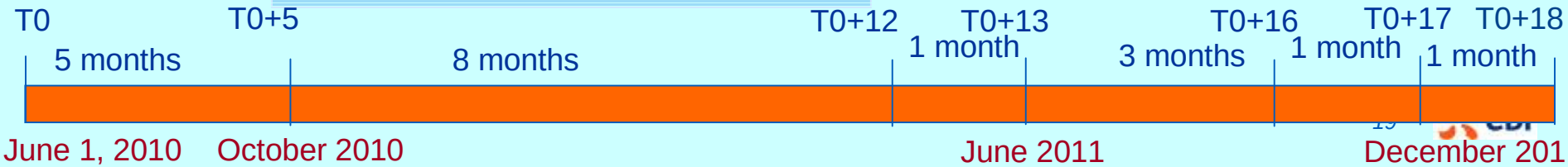
Weather, Climatology and Earth Sciences

Chair: Giovanni Aloisio / ENES-CMCC

Vice-Chair: Massimo Cocco/ INGV



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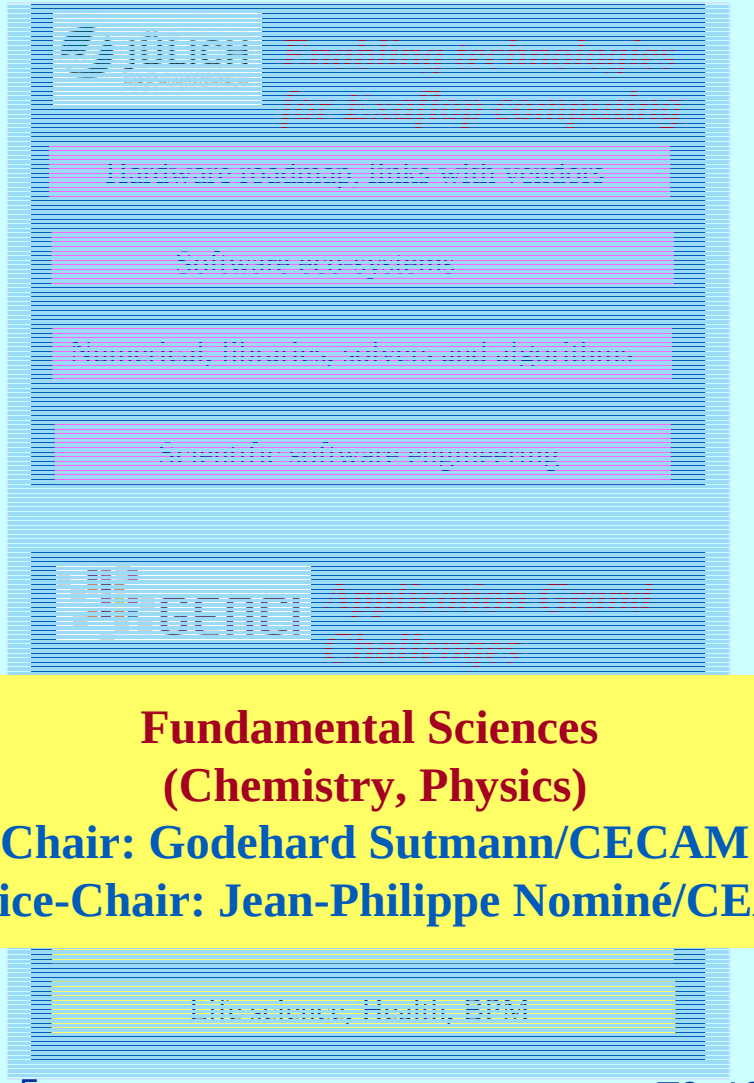
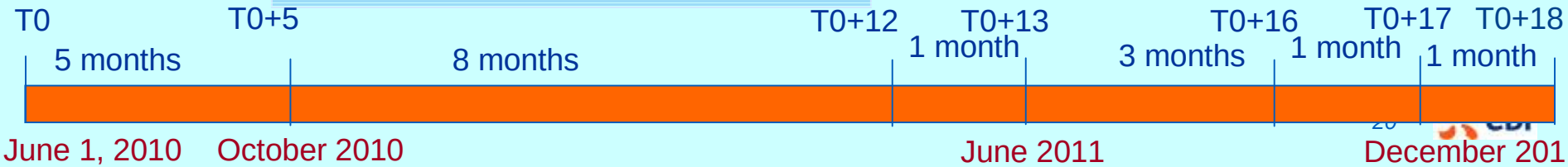


Fundamental Sciences
(Chemistry, Physics)
Chair: Godehard Sutmann/CECAM
Vice-Chair: Jean-Philippe Nominé/CEA



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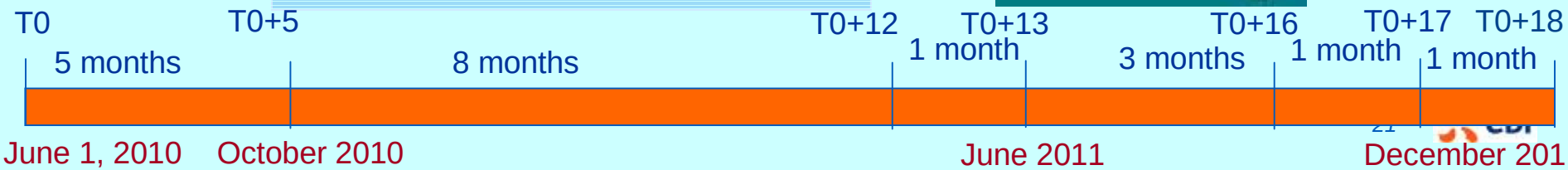
Life science, Health, BPM
Chair: Modesto Orozco/ BSC
Vice-Chair: Janet Thorton/EMBL-EBI



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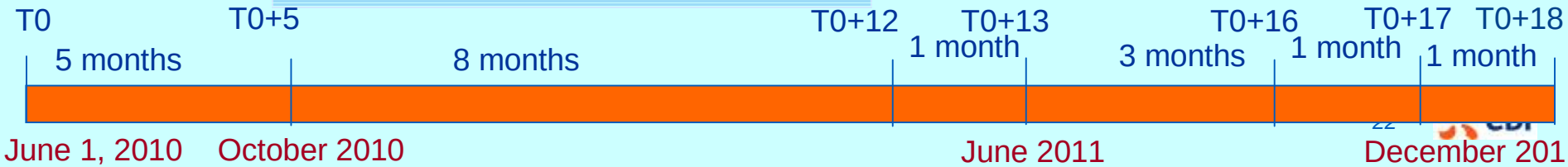
Hardware roadmap, links with Vendors

Chair: Herbert Huber/STRATOS-LRZ

Vice-Chair: Sanzio Bassini/CINECA



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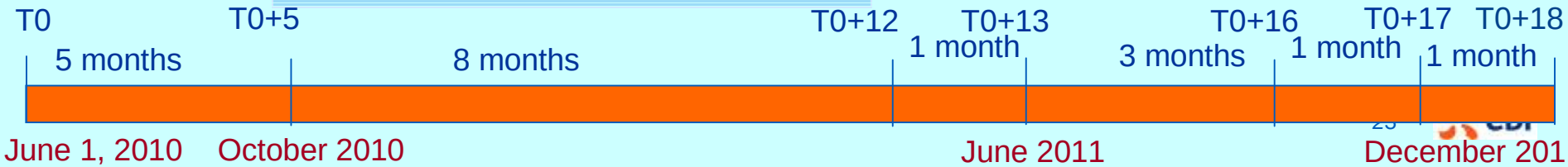
INRIA

JÜLICH



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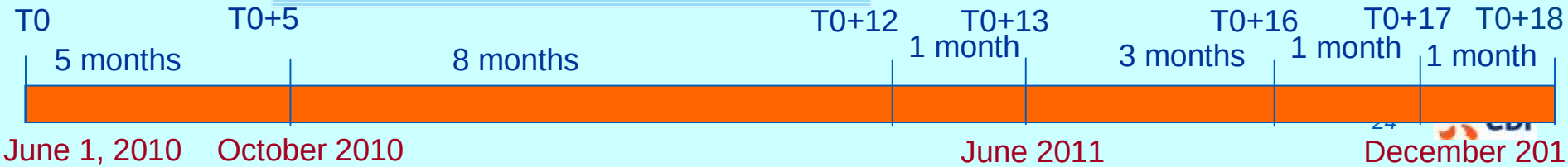
Numerical, libraries, solvers and algorithms
Chair: Iain Duff/ STFC-Rutherford Appleton Laboratory
Vice-Chair: Andreas Grothey/ Edinburgh University

Science & Technology Facilities Council
Rutherford Appleton Laboratory



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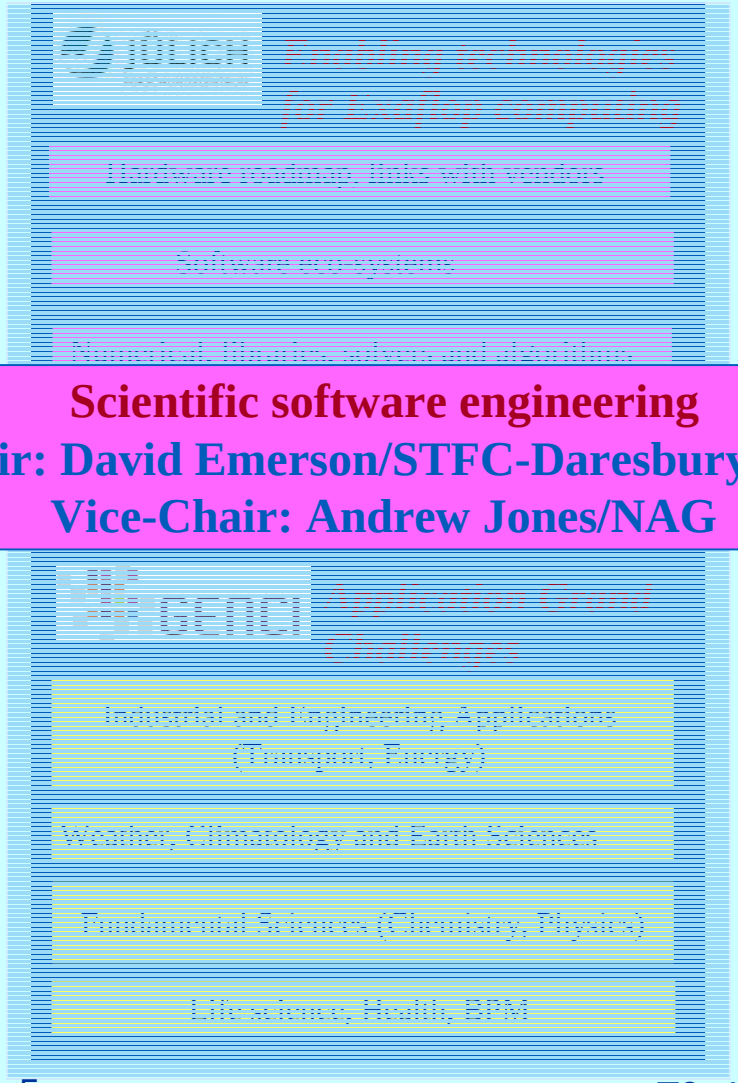
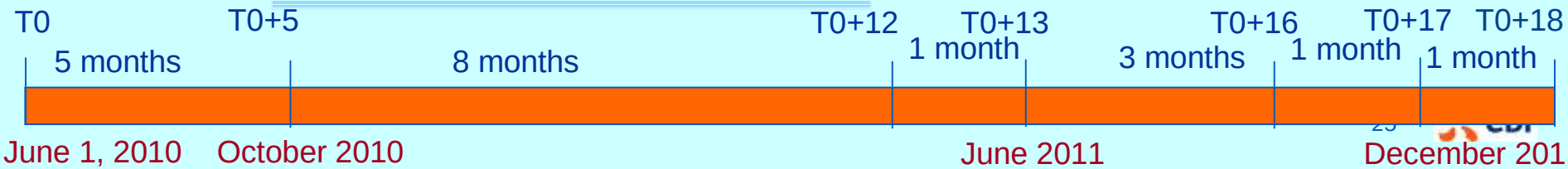


Scientific software engineering
Chair: David Emerson/STFC-Daresbury Lab.
Vice-Chair: Andrew Jones/NAG



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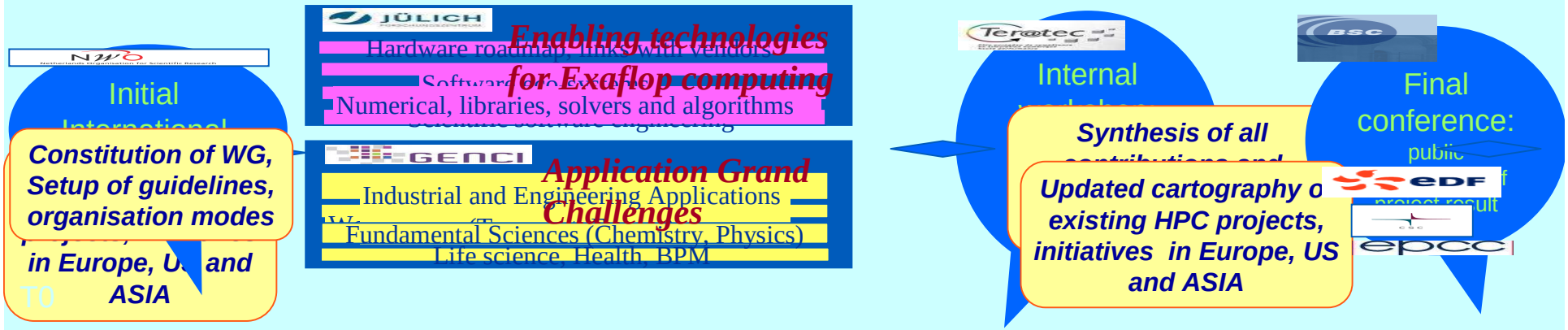
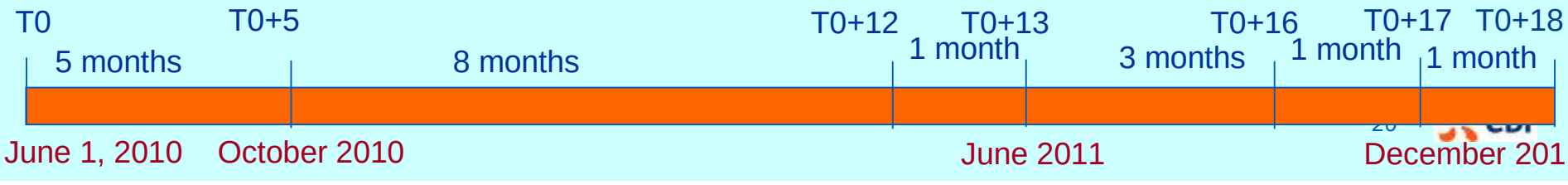
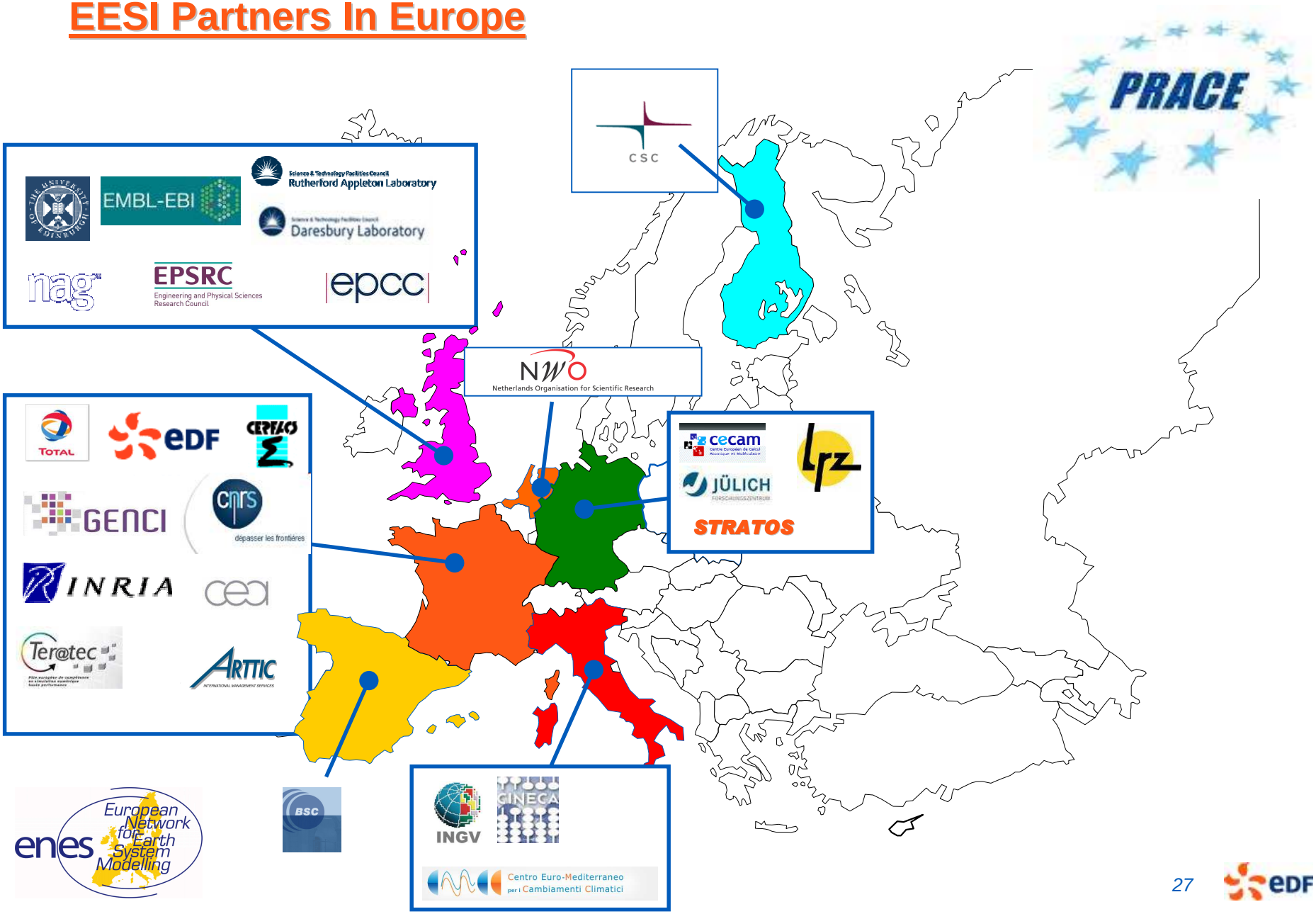
Link with US and ASIA

Joint IESP/EESI workshops: present EESI Working Groups outputs, include inputs from US and ASIA, identification of US, ASIA and European cross actions





EESI Partners In Europe



EESI Partners around the world